

The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

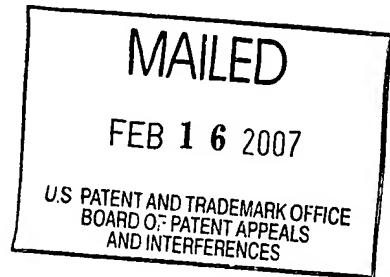
UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MARC CHASON, JANICE DANVIR, JING QI,
and NADIA YALA

Appeal 2006-2590
Application 10/044,777
Technology Center 2800

Decided: February 16, 2007



Before LANCE LEONARD BARRY, HOWARD B. BLANKENSHIP, and ALLEN R. MACDONALD, Administrative *Patent Judges*.

BLANKENSHIP, *Administrative Patent Judge*.

DECISION ON APPEAL

This appeal involves claims 1-28, the only claims pending in this application. We have jurisdiction over the appeal pursuant to 35 U.S.C. § 6(b).

INTRODUCTION

The claims are directed to semiconductor packages in which an interposer is provided between a semiconductor die and the substrate. Claim 1 is illustrative:

1. A method comprising:

providing an interposer having at least one semiconductor die attached to a first side thereof;

prior to placing the interposer on a printed wiring board, disposing a non-conductive underfill material on at least a portion of a second side thereof.

The Examiner relies on the following prior art references to show unpatentability:

Grube	EP 0475022 A1	Mar. 18, 1992
Spigarelli	US 5,251,266	Oct. 5, 1993
Lin	US 5,258,648	Nov. 2, 1993
Capote	US 6,335,571 B1	Jan. 1, 2002

The rejections as presented by the Examiner are as follows:

1. Claims 1-13 and 21-28 are rejected under 35 U.S.C. § 103(a) as unpatentable over Lin and Capote.
2. Claims 14-18 are rejected under 35 U.S.C. § 103(a) as unpatentable over Lin, Capote, and Grube.
3. Claims 19 and 20 are rejected under 35 U.S.C. § 103(a) as unpatentable over Lin, Capote, Grube, and Spigarelli.

OPINION

I. Pierce

The Examiner applied Pierce (US 2002/0119600 A1) against the claims in a non-final rejection mailed October 28, 2002. Appellants in response filed (Feb. 5, 2003) a Rule 131 affidavit to antedate Pierce, which has a U.S. filing date of February 23, 2001. The Examiner withdrew the rejections over Pierce in a rejection mailed April 21, 2003, contending that Appellants' paper was sufficient to remove Pierce as a reference.

37 C.F.R. § 1.131(b) (2006) provides:

[§ 1.131 Affidavit or declaration of prior invention.]

(b) The showing of facts shall be such, in character and weight, as to establish reduction to practice prior to the effective date of the reference, or conception of the invention prior to the effective date of the reference coupled with due diligence from prior to said date to a subsequent reduction to practice or to the filing of the application. Original exhibits of drawings or records, or photocopies thereof, must accompany and form part of the affidavit or declaration or their absence must be satisfactorily explained.

The affidavit filed February 5, 2003 by Appellants is deficient at least for the reasons that: (1) the affidavit is signed by less than all the named inventors, without any showing that less than all the named inventors invented the subject matter of the claims under rejection (*see Manual of Patent Examining Procedure* § 715.04 (8th Ed., Rev. 5, Aug. 2006)); (2) the affiant does not specify where, and explain how, the attached evidence shows conception of the invention prior to the effective date of the reference; and (3) the affiant does not allege, let alone show, due diligence

from prior to the effective date of the reference to a subsequent reduction to practice or to the filing of the application.

In the event of further prosecution in this or a continuing application, the Examiner should re-evaluate Pierce vis-à-vis the subject matter that is claimed.

II. The Standing Rejections

Lin teaches that underfill materials were conventionally used between a flip chip device and a substrate. Use of the material reduced the potential for open connections, but prohibited rework. If such an underfill material were used, it was not possible to remove a defective semiconductor device from the substrate and replace the defective part with a functional part. Lin col. 2, ll. 39-65. On the other hand, an underfill material between an interposer and the substrate does not prevent a defective semiconductor die from being removed and replaced. Col. 4, ll. 1-19. Lin's contribution to the art includes a rigid interposer 22 (Fig. 1) attached to semiconductor die 12 such that solder bumps 16 align with, and are in electrical contact with, a plurality of electrical vias 24 in the interposer. *Id.*, ll. 49-55. Rather than placing an underfill material between the die and the substrate, Lin teaches placing an underfill material 36 between the interposer 22 and the substrate (e.g., PC board 34), as depicted in Figure 4. The arrangement allows the semiconductor die 12 to be removed should rework be necessary. Col. 5, ll. 21-41.

Lin thus describes the subject matter of instant claim 1, but does not expressly set forth that the underfill material is placed on the interposer "prior to placing the interposer on a printed wiring board."

Capote describes, in columns 1 through 3, numerous problems with prior art processes and products relating to underfill materials between flip chip devices and substrates. Capote teaches a need in the art to pre-apply an underfill material to fill completely the gap between a chip and substrate in such a way that, *inter alia*, the coefficient of expansion of the material in the gap is near that of the solder. Capote col. 4, ll. 10-15. The reference teaches a solder bumped chip or substrate with an encapsulant pre-attached, which may consist of two or more layers performing a distinct function. Col. 6, ll. 19-29. Capote describes several embodiments in which either the substrate or the chip may be pre-coated with the encapsulant for filling the gap between the chip and substrate. *E.g.*, col. 11, ll. 9-32.

Capote thus teaches the pre-coating of underfill material on at least one of the surfaces that will bear the underfill material in the finished product. The references would thus have suggested, to one skilled in the art, to pre-coat an interposer as described by Lin with an underfill material prior to placing the interposer on a printed wiring board.

Appellants advance several arguments in support of the belief that the references fail to support a conclusion of *prima facie* obviousness of the subject matter of claim 1. We have considered all the arguments that are properly before us, but we need not address those arguments that are not commensurate with what the claim actually requires. It is the *claims* that measure the invention. *SRI Int'l v. Matsushita Elec. Corp.*, 775 F.2d 1107, 1121, 227 USPQ 577, 585 (Fed. Cir. 1985) (en banc).

Appellants argue that Capote notes, in the background discussion in columns 1 and 2, the prior art use of interposers and teaches therein that interposers are to be used *without* an underfill material. As such, Appellants

contend that the artisan would not be led to move in a fashion “contrary to the explicit teachings” of Capote. (Br. 5-6.)

Aside from the flaws in the position that the Examiner points out in the Answer, we find that Capote discusses prior art interposers made of flexible circuitry between the chips and solder joints. The flex circuit, having air gaps around the solder joints, undergoes expansion and contraction without distorting the solder joints. Capote col. 1, ll. 60-67; col. 2, ll. 18-20. Capote thus discusses prior art flexible interposers having air gaps around the solder joints. Capote does not address the type of rigid interposer, associated with an underfill material having no air gaps around the solder joints that interface with the substrate, described by Lin. The solder joints and air gaps discussed by Capote refer to air gaps 103 (Fig. 3) around solder joints 104, which attach to substrate 101. *See* Capote col. 1, ll. 36-59. Moreover, the preferred rigid interposer described by Lin consists of a material having a coefficient of thermal expansion that closely approximates that of the semiconductor die (col. 6, ll. 28-60), in opposition to flexible circuitry that functions as an interposer.

We are not persuaded that Capote teaches that prior art interposers, as taught by Lin, represent an alternative approach to its teachings with respect to underfill materials. We are thus not persuaded, as Appellants allege, that Capote’s teachings are solely directed to the use of underfill materials between chips and substrates.

Appellants also submit (Br. 6) that “Lin teaches that an underfill material can be added between an interposer and a substrate *following* a combination of the two.” Appellants do not point out where this alleged teaching resides in Lin. As we have indicated *supra*, Lin does not express

when the underfill material is to be added. At best, Lin might suggest that the underfill material may be added between an interposer and a substrate following the combination of the two; the reference could be read as describing *prior art* placement of an underfill after a *flip chip device* is mounted to a substrate (col. 2, ll. 39-45).¹ In any event, the rejection relies on Capote, not Lin, for the “prior to” limitation of instant claim 1.

Appellants’ further remarks in the Reply Brief in defense of claim 1 seem to suggest that the broad terms somehow distinguish over the use of two (or more) layers of underfill material that are taught in embodiments of Capote. The claim, however, requires no more than that a non-conductive underfill material be disposed, prior to placing the interposer on a printed wiring board, on at least a portion of a side of the interposer apart from that to which at least one semiconductor die is attached. The claim does not preclude, for example, that underfill material also be placed on the substrate (i.e., printed wiring board), or that additional layers of underfill material be added to the interposer.

Appellants’ remarks in the Reply Brief also seem to ignore the fact that Capote teaches that an air gap is detrimental to solder joints between materials having relatively different rates of thermal expansion. Capote col. 1, ll. 36-67. The teaching of pre-coating underfill material in Capote applies to the interface between an interposer and PC board as taught by Lin -- not to the interface between the die and interposer, which Lin teaches to have

¹ We acknowledge that the Examiner finds that Lin teaches a capillary-flown underfill between the interposer and the substrate (Answer 14), but the Examiner does not specify where Lin contains the teaching.

approximately the same coefficient of thermal expansion, thus avoiding the solder joint fatigue associated with air gaps that is identified by Capote.

We are thus not persuaded of error in the § 103 rejection of claim 1. Claims 14-20, not separately argued, fall with claim 1.

In response to the rejection of claim 2, Appellants acknowledge (Br. 7) that Lin discloses an interposer having interface electrodes disposed between itself and the substrate to which it is attached and which electrodes are on the same side of the interposer as the side where the underfill material is added. Appellants argue that Lin only teaches that underfill material should be added after mounting the interposer on a substrate, which ignores the teachings of Capote. Appellants do not show error in the Examiner's findings (e.g., Answer 6-7) as to how Capote teaches a pre-form underfill on surfaces having at least one interface electrode. Even assuming that the combination would have suggested greater difficulty in assembly, as alleged by Appellants in the Reply Brief, the recognition of a more difficult assembly would not necessarily outweigh the known advantages in the combination as evidenced by Capote and Lin. Appellants have not provided any evidence in support of the allegation. Arguments of counsel are not evidence. *See, e.g., Meitzner v. Mindick*, 549 F.2d 775, 782, 193 USPQ 17, 22 (CCPA 1977); *In re Pearson*, 494 F.2d 1399, 1405, 181 USPQ 641, 646 (CCPA 1974). We thus sustain the rejection of claim 2.

The remainder of Appellants' remarks in the Brief merely refer to claims and make general allegations of patentability, without addressing the Examiner's findings in the Final Rejection. We find none of the remarks to be persuasive of error in the rejection.

Appellants submit new arguments in the Reply Brief (page 5). However, the Examiner pointed to the sections of the references on which the rejections relied in the Final Rejection; Appellants could have presented the arguments in the Brief, thus allowing us the opportunity to evaluate the arguments in light of the Examiner's response in the Answer.² We thus consider the arguments at page 5 of the Reply Brief to be untimely for the purposes of this proceeding. We will not consider or address the new arguments in this opinion.³

DECISION

In summary, we sustain the rejection of claims 1-28 under 35 U.S.C § 103(a).

AFFIRMED

APJ Initials:

HBB

LLB

ARM

PC/GW:

² At the time of submission of the Reply Brief, the Examiner could not respond to arguments in a reply brief without withdrawing the final rejection and reopening prosecution to respond to the reply brief. *See* 37 C.F.R. § 1.193(b) (1) (2004).

³ Moreover, the new arguments appear answered by the views expressed in this opinion, although we have not addressed the seeming confusion between facts within the personal knowledge of an examiner, which are treated by 37 C.F.R. § 1.104(d)(2) (2004), and the taking of official notice (e.g., *In re Ahlert*, 424 F.2d 1088, 1091, 165 USPQ 418, 420 (CCPA 1970); *In re Boon*, 439 F.2d 724, 728, 169 USPQ 231, 234 (CCPA 1971)).

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